



# Multiple-Output Network Clock Generator

MAX9489

## General Description

The MAX9489 clock generator provides multiple clock outputs, ideal for network routers. The MAX9489 provides 15 buffered clock outputs, each independently programmable to any of 10 individual frequencies: 133MHz, 125MHz, 100MHz, 83MHz, 80MHz, 66MHz, 62.5MHz, 50MHz, 33MHz, or 25MHz. All of the outputs are single-ended LVCMOS. The MAX9489 is controlled through its I<sup>2</sup>C™ interface.

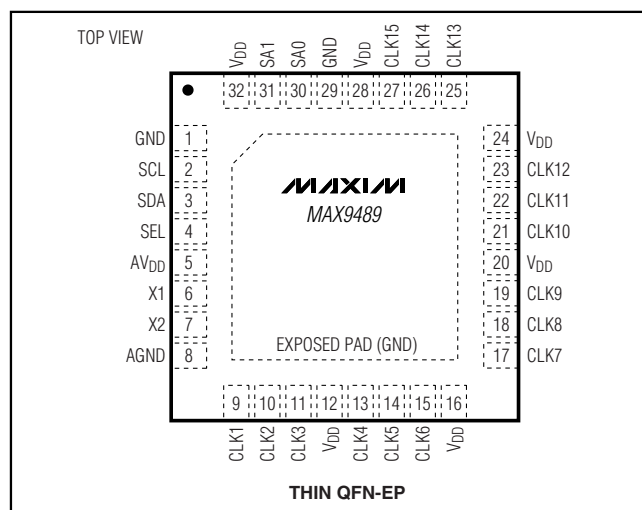
At power-up, the frequency of output CLK1 is set by the tri-level input SEL to 100MHz, 125MHz, or 133MHz, while all other outputs are logic low. All outputs are then programmable to any available frequency through the I<sup>2</sup>C interface. Additionally, all output frequencies are adjustable up or down, by a margin of 5% or 10%, through the I<sup>2</sup>C interface.

The MAX9489 requires a 25MHz reference that can be either a crystal or an external clock signal. The MAX9489 requires a +3.0V to +3.6V power supply and is available in a 32-pin thin QFN package with an exposed pad for heat removal.

## Applications

- Network Routers
- Telecom/Networking Equipment
- Storage Area Networks/Network Attached Storage

## Pin Configuration



I<sup>2</sup>C is a trademark of Philips Corp.  
Purchase of I<sup>2</sup>C components of Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

## Features

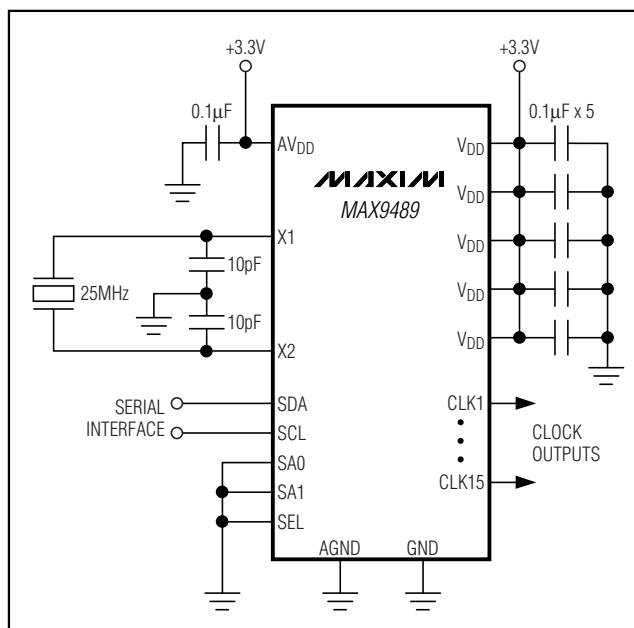
- ◆ 15 LVCMOS Outputs with 10 Independently Programmable Frequencies: 133MHz, 125MHz, 100MHz, 83MHz, 80MHz, 66MHz, 62.5MHz, 50MHz, 33MHz, and 25MHz
- ◆ 25MHz Crystal or Clock Input Reference
- ◆ Programmable Through I<sup>2</sup>C Interface
- ◆ Programmable Output Frequency Margin of ±5% or ±10%
- ◆ Pin-Selectable Power-Up Frequency for CLK1 Output: 100MHz, 125MHz, or 133MHz
- ◆ Low Output Period Jitter: < 48ps<sub>RMS</sub>
- ◆ Output-to-Output Skew < 200ps
- ◆ Available in 32-Lead, 5mm x 5mm x 0.8mm, Thin QFN Package
- ◆ Operates from +3.0V to +3.6V Power Supply
- ◆ Power Dissipation 450mW (typ)
- ◆ Extended Temperature Range: -40°C to +85°C

## Ordering Information

| PART       | TEMP RANGE     | PIN-PACKAGE                          |
|------------|----------------|--------------------------------------|
| MAX9489ETJ | -40°C to +85°C | 32 Thin QFN-EP*<br>5mm x 5mm x 0.8mm |

\*EP = Exposed pad.

## Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

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## ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub> to GND .....-0.3V to +4.0V  
 AGND to GND .....-0.3V to +0.3V  
 All Other Pins to GND .....-0.3V to (V<sub>DD</sub> + 0.3V)  
 Short-Circuit Duration for all CLK\_ Outputs .....Continuous  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
     32-Pin Thin QFN (derate 21.3mW/°C above +70°C) ....1702mW

Storage Temperature Range .....-65°C to +150°C  
 Maximum Junction Temperature .....+150°C  
 Operating Temperature Range .....-40°C to +85°C  
 ESD Rating (Human Body Model) .....±2kV  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = AV<sub>DD</sub> = +3.0V to +3.6V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>DD</sub> = AV<sub>DD</sub> = +3.3V, T<sub>A</sub> = +25°C.)  
 (Note 1)

| PARAMETER                                   | SYMBOL                              | CONDITIONS   | MIN                   | TYP | MAX                   | UNITS |
|---|-------------------------------------|--|-----------------------|-----|-----------------------|-------|
| <b>CLOCK INPUT (X1)</b>                     |                                     |  |                       |     |                       |       |
| Input High Level                            | V <sub>IH1</sub>                    |  | 2.0                   |     |                       | V     |
| Input Low Level                             | V <sub>IL1</sub>                    |  |                       |     | 0.8                   | V     |
| Input Current                               | I <sub>IL1</sub> , I <sub>IH1</sub> | V <sub>X_</sub> = 0 to V <sub>DD</sub>                     | -5                    |     | +5                    | μA    |
| <b>CLOCK OUTPUTS (CLK_)</b>                 |                                     |  |                       |     |                       |       |
| Output High Level                           | V <sub>OH</sub>                     | I <sub>OH</sub> = -100μA                                   | V <sub>DD</sub> - 0.2 |     |                       | V     |
|   |                                     | I <sub>OH</sub> = -4mA                                     | 2.4                   |     |                       |       |
|   |                                     | I <sub>OH</sub> = -8mA                                     | 2.1                   |     |                       |       |
| Output Low Level                            | V <sub>OL</sub>                     | I <sub>OL</sub> = 100μA                                    |                       |     | 0.2                   | V     |
|   |                                     | I <sub>OL</sub> = 4mA                                      |                       |     | 0.4                   |       |
|   |                                     | I <sub>OL</sub> = 8mA                                      |                       |     | 0.75                  |       |
| Output Short-Circuit Current                | I <sub>OS</sub>                     | CLK_ = V <sub>DD</sub> or GND                              |                       |     | 45                    | mA    |
| Output Capacitance                          | C <sub>O</sub>                      | (Note 2)   |                       |     | 5                     | pF    |
| <b>TRI-LEVEL INPUTS (SEL, SA0, SA1)</b>     |                                     |  |                       |     |                       |       |
| Input High Level                            | V <sub>IH2</sub>                    |  | 2.5                   |     |                       | V     |
| Input Low Level                             | V <sub>IL2</sub>                    |  |                       |     | 0.8                   | V     |
| Input Open Level                            | V <sub>IO2</sub>                    |  | 1.35                  |     | 1.90                  | V     |
| Input Current                               | I <sub>IL2</sub> , I <sub>IH2</sub> | V <sub>IL2</sub> = 0 or V <sub>IH2</sub> = V <sub>DD</sub> | -10                   |     | +10                   | μA    |
| <b>SERIAL INTERFACE (SCL, SDA) (Note 3)</b> |                                     |  |                       |     |                       |       |
| Input High Level                            | V <sub>IH</sub>                     |  | 0.7 x V <sub>DD</sub> |     | V <sub>DD</sub>       | V     |
| Input Low Level                             | V <sub>IL</sub>                     |  | 0                     |     | 0.3 x V <sub>DD</sub> | V     |
| Input leakage Current                       | I <sub>IH</sub> , I <sub>IL</sub>   |  | -1                    |     | +1                    | μA    |
| Low-Level Output                            | V <sub>OL</sub>                     | I <sub>SINK</sub> = 4mA                                    | 0                     |     | 0.4                   | V     |
| Input Capacitance                           | C <sub>i</sub>                      | (Note 2)   |                       |     | 10                    | pF    |

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## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = AV_{DD} = +3.0V$  to  $+3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{DD} = AV_{DD} = +3.3V$ ,  $T_A = +25^{\circ}C$ .) (Note 1)

| PARAMETER                    | SYMBOL    | CONDITIONS                                     | MIN | TYP | MAX | UNITS |
|------------------------------|-----------|--|-----|-----|-----|-------|
| <b>POWER SUPPLIES</b>        |           |  |     |     |     |       |
| Digital Power-Supply Voltage | $V_{DD}$  |  | 3.0 |     | 3.6 | V     |
| Analog Power-Supply Voltage  | $AV_{DD}$ |  | 3.0 |     | 3.6 | V     |
| Total Supply Current         |           | $C_L = 10pF$ (with all CLK_ outputs at 133MHz) |     | 134 | 160 | mA    |
| Total Power-Down Current     | $I_{PD}$  | All clock registers = 0x00                     |     | 38  | 47  | mA    |

## AC ELECTRICAL CHARACTERISTICS

( $V_{DD} = AV_{DD} = +3.0V$  to  $+3.6V$ ,  $C_L = 10pF$ , unless otherwise noted. Typical values are at  $V_{DD} = AV_{DD} = +3.3V$ ,  $T_A = +25^{\circ}C$ , with all CLK\_ outputs at 133MHz.) (Note 2)

| PARAMETER                   | SYMBOL       | CONDITIONS                            | MIN | TYP | MAX | UNITS   |
|-----------------------------|--------------|---------------------------------------|-----|-----|-----|---------|
| <b>OUTPUTS (CLK_)</b>       |              |                                       |     |     |     |         |
| Crystal Frequency Tolerance | $\Delta f_A$ |                                       | -50 |     | +50 | ppm     |
| Output-to-Output Skew       | $t_{SKO}$    | Any two CLK_ outputs                  |     |     | 200 | ps      |
| Rise Time                   | $t_{R1}$     | 20% $V_{DD}$ to 80% $V_{DD}$          |     | 1.8 | 2.5 | ns      |
| Fall Time                   | $t_{F1}$     | 80% $V_{DD}$ to 20% $V_{DD}$          |     | 1.8 | 2.5 | ns      |
| Duty Cycle                  |              |                                       | 40  |     | 60  | %       |
| Output Period Jitter        | $J_P$        | RMS                                   |     | 53  |     | ps      |
| Power-Up Time               | $t_{PO}$     | $V_{DD} > 2.8V$ to PLL lock           |     | 2   |     | ms      |
| PLL Lockup Time             | $t_{Lock}$   | PLL dividing ratio set to PLL lock    |     | 20  |     | $\mu s$ |
| Margin Accuracy             |              | Select $\pm 5\%$ or $\pm 10\%$ margin | -1  |     | +1  | %       |

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## SERIAL INTERFACE TIMING

(V<sub>DD</sub> = AV<sub>DD</sub> = +3.3V, T<sub>A</sub> = -40°C to +85°C.) (Note 1, Figure 2)

| PARAMETER                                       | SYMBOL              | CONDITIONS   | MIN                       | TYP | MAX | UNITS |
|---|---------------------|--------------|---------------------------|-----|-----|-------|
| Serial Clock                                    | f <sub>SCL</sub>    |              |                           |     | 400 | kHz   |
| Bus Free Time Between STOP and START Conditions | t <sub>BUF</sub>    |              | 1.3                       |     |     | μs    |
| Hold Time, Repeated START Condition             | t <sub>HD,STA</sub> |              | 0.6                       |     |     | μs    |
| Repeated START Condition Setup Time             | t <sub>SU,STA</sub> |              | 0.6                       |     |     | μs    |
| STOP Condition Setup Time                       | t <sub>SU,STO</sub> |              | 0.6                       |     |     | μs    |
| Data Hold Time Master                           | t <sub>HD,DAT</sub> | (Note 4)     | 15                        |     | 900 | ns    |
| Data Hold Time Slave                            | t <sub>HD,DAT</sub> | (Note 4)     | 15                        |     | 900 | ns    |
| Data Setup Time                                 | t <sub>SU,DAT</sub> |              | 100                       |     |     | ns    |
| SCL Clock Low Period                            | t <sub>LOW</sub>    |              | 1.3                       |     |     | μs    |
| SCL Clock High Period                           | t <sub>HIGH</sub>   |              | 0.7                       |     |     | μs    |
| Rise Time of SDA and SCL, Receiving             | t <sub>R</sub>      | (Notes 2, 5) | 20 +<br>0.1C <sub>b</sub> |     | 300 | ns    |
| Fall Time of SDA and SCL, Receiving             | t <sub>F</sub>      | (Notes 2, 5) | 20 +<br>0.1C <sub>b</sub> |     | 300 | ns    |
| Fall Time of SDA, Transmitting                  | t <sub>F,TX</sub>   | (Notes 2, 5) | 20 +<br>0.1C <sub>b</sub> |     | 250 | ns    |
| Pulse Width of Spike Suppressed                 | t <sub>SP</sub>     | (Notes 2, 6) | 0                         |     | 50  | ns    |
| Capacitive Load for Each Bus Line               | C <sub>b</sub>      | (Note 2)     |                           |     | 400 | pF    |

**Note 1:** All DC parameters tested at T<sub>A</sub> = +25°C. Specifications over temperature are guaranteed by design.

**Note 2:** Guaranteed by design.

**Note 3:** No high output level is specified but only the output resistance to the bus. For I<sup>2</sup>C, the high-level voltage is provided by pullup resistors on the bus.

**Note 4:** A master device must provide a hold time of at least 300ns for the SDA signal (referred to V<sub>IL</sub> of the SCL signal) to bridge the undefined region of SCL's falling edge.

**Note 5:** C<sub>b</sub> = total capacitance of one bus line in pF. t<sub>R</sub> and t<sub>F</sub> measured between 0.3(V<sub>DD</sub>) and 0.7(V<sub>DD</sub>).

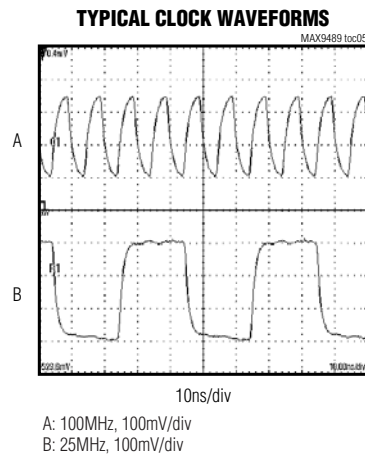
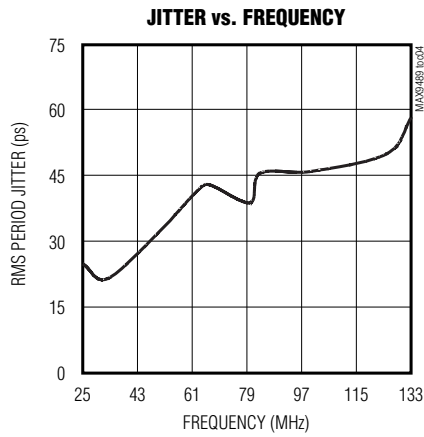
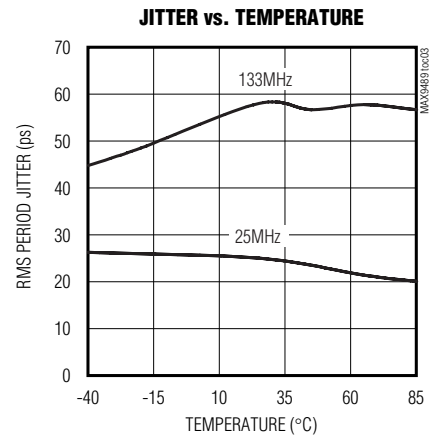
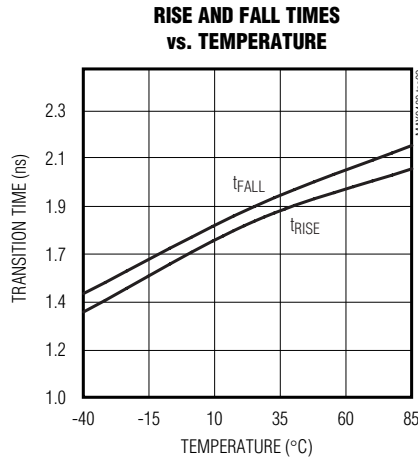
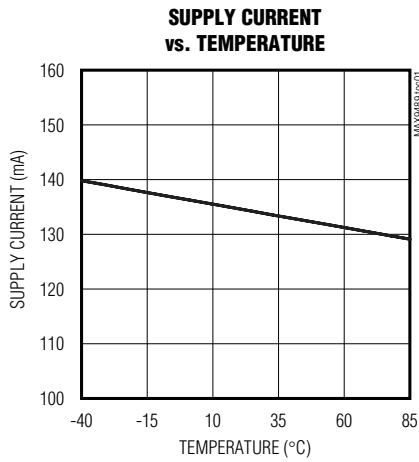
**Note 6:** Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

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## Typical Operating Characteristics

( $V_{DD} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

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## Pin Description

| PIN                    | NAME  | FUNCTION  |
|------------------------|-------|---|
| 1, 29                  | GND   | Digital Ground  |
| 2                      | SCL   | Serial Clock Input. Serial interface clock.   |
| 3                      | SDA   | Serial Data I/O. Data I/O of serial interface.  |
| 4                      | SEL   | Frequency Select for CLK1. Selects the frequency for CLK1 at power-up. SEL is a tri-level input. Force SEL high for CLK1 = 100MHz. Leave SEL open for CLK1 = 125MHz. Force SEL low for CLK1 = 133MHz.               |
| 5                      | AVDD  | Power-Supply Input for Analog Circuits  |
| 6                      | X1    | Crystal Connection or Clock Input. If using a 25MHz crystal, connect it to X1 and X2. If using a reference clock, connect the clock signal to X1, and leave X2 floating. See the <i>Typical Operating Circuit</i> . |
| 7                      | X2    |   |
| 8                      | AGND  | Analog GND  |
| 9                      | CLK1  | Clock 1 Output  |
| 10                     | CLK2  | Clock 2 Output  |
| 11                     | CLK3  | Clock 3 Output  |
| 12, 16, 20, 24, 28, 32 | VDD   | Power-Supply Input for Digital Circuits   |
| 13                     | CLK4  | Clock 4 Output  |
| 14                     | CLK5  | Clock 5 Output  |
| 15                     | CLK6  | Clock 6 Output  |
| 17                     | CLK7  | Clock 7 Output  |
| 18                     | CLK8  | Clock 8 Output  |
| 19                     | CLK9  | Clock 9 Output  |
| 21                     | CLK10 | Clock 10 Output   |
| 22                     | CLK11 | Clock 11 Output   |
| 23                     | CLK12 | Clock 12 Output   |
| 25                     | CLK13 | Clock 13 Output   |
| 26                     | CLK14 | Clock 14 Output   |
| 27                     | CLK15 | Clock 15 Output   |
| 30                     | SA0   | Address-Select Inputs for Serial Interface. SA0 and SA1 select the serial interface address, as shown in Table 1. SA0 and SA1 are tri-level inputs, making nine possible address combinations.                      |
| 31                     | SA1   |   |
| EP                     | —     | Exposed pad. Connect to GND.  |

# Multiple-Output Network Clock Generator

## Detailed Description

The MAX9489 clock generator produces 15 clock signals, CLK1 through CLK15. Each output is programmable through control registers to any of 10 individual frequencies: 133MHz, 125MHz, 100MHz, 83MHz, 80MHz, 66MHz, 62.5MHz, 50MHz, 33MHz, or 25MHz. Additionally, the frequency of all outputs can be changed  $\pm 5\%$  or  $\pm 10\%$  through the frequency-margin control register. At power-up, the frequency of CLK1 is pin programmable to 100MHz, 125MHz, or 133MHz, and all other CLK outputs are logic low. The required 25MHz input reference frequency can be either a crystal or an external clock signal. Figure 1 shows the MAX9489 functional block diagram.

The MAX9489 is programmed through its I<sup>2</sup>C serial interface. The I<sup>2</sup>C address is selected with two, tri-level inputs, allowing up to nine MAX9489 devices to share the same I<sup>2</sup>C bus. Power-supply and logic interface signals are +3.0V to +3.6V. The operating state of the MAX9489 is set by writing to the control registers, and read by reading the control registers.

## Reference Frequency Input

A reference frequency is required for the MAX9489. The reference can be a 25MHz crystal or an external clock signal. If using a 25MHz crystal, connect it across X1 and X2, and connect 10pF capacitors from X1 and

X2 to GND (see the *Typical Operating Circuit*). If using an external clock, connect the signal to X1 and leave X2 floating.

## Serial Interface

The MAX9489 is programmed through its I<sup>2</sup>C serial interface. This interface has a clock, SCL, and a bidirectional data line, SDA. In an I<sup>2</sup>C system, a master, typically a microcontroller, initiates all data transfers to and from slave devices, and generates the clock to synchronize the data transfers.

The MAX9489 operates as a slave device. The timing of the SDA and SCL signals is detailed in Figure 2, the *Serial Interface Timing* diagram. SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7k $\Omega$ , is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7k $\Omega$ , is required on SCL if there are multiple masters on the 2-wire bus, or if the master in a single-master system has an open-drain SCL output.

## Bit Transfer

One data bit is transferred during each SCL clock cycle. SDA must remain stable during the high period of SCL, because changes in SDA while SCL is high are START and STOP control signals. Both SDA and SCL idle high.

## START and STOP Conditions

A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 2). When communication is complete, a master issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

## Acknowledge Bits

After each 8 bits transferred, the receiving device generates an acknowledge signal by pulling SDA low for the entire duration of the 9th clock pulse. If the receiving device does not pull SDA low, a not-acknowledge is indicated (Figure 3).

## Device Address

The MAX9489 has a 7-bit device address, pin configured by the two tri-level address inputs SA1 and SA0. To select the device address, connect SA1 and SA0 to V<sub>DD</sub>, GND, or leave open, as indicated in Table 1. The MAX9489 has nine possible addresses, allowing up to nine MAX9489 devices to share the same interface bus.

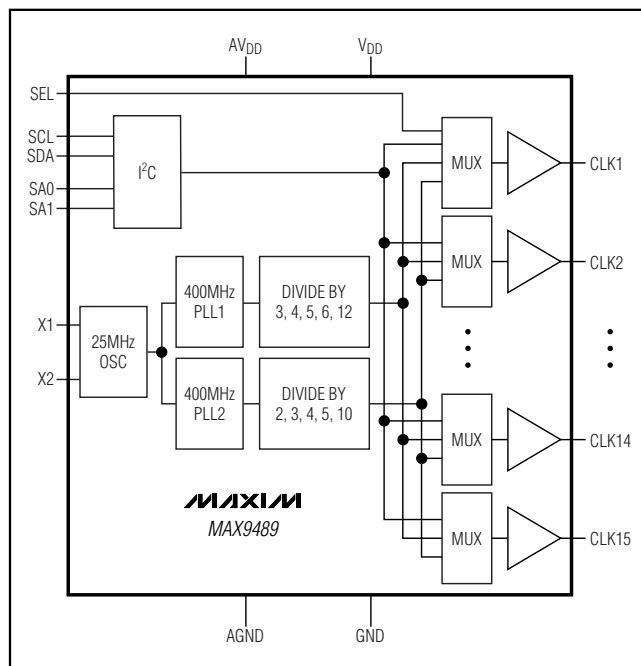


Figure 1. MAX9489 Functional Diagram

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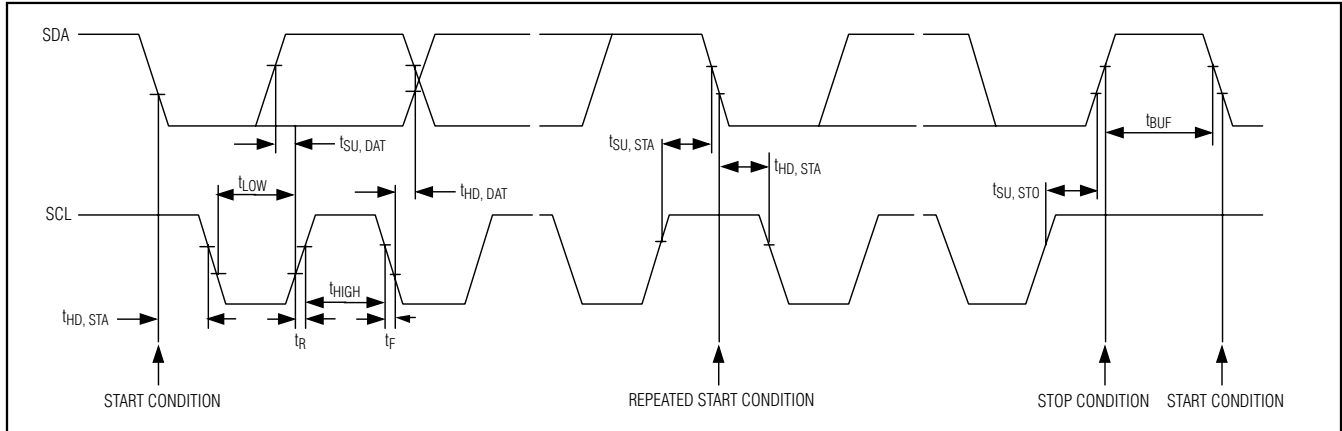


Figure 2. Serial Interface Timing

Table 1. Device I<sup>2</sup>C Address Selection

| PIN             |                 | DEVICE ADDRESS |
|-----------------|-----------------|----------------|
| SA1             | SA0             |                |
| Open            | V <sub>DD</sub> | 110 0010       |
| Open            | GND             | 110 0100       |
| Open            | Open            | 110 1000       |
| GND             | V <sub>DD</sub> | 111 0000       |
| GND             | GND             | 110 1001       |
| GND             | Open            | 110 1100       |
| V <sub>DD</sub> | V <sub>DD</sub> | 111 0100       |
| V <sub>DD</sub> | GND             | 111 0010       |
| V <sub>DD</sub> | Open            | 111 0001       |

### Writing to the MAX9489

Writing to the MAX9489 begins with a START condition (Figures 3 and 4). Following the START condition, each pulse on SCL transfers 1 bit of data. The first 7 bits comprise the device address (see the *Device Address* section). The 8th bit is low to indicate a write operation. An acknowledge bit is then generated by the MAX9489, signaling that it recognizes its address. The next 8 bits form the register address byte (Table 2) and determine which control register will receive the following data byte. The MAX9489 then generates another acknowledge bit. The data byte is then written into the addressed register of the MAX9489. An acknowledge bit by the MAX9489 followed by a required STOP condition by the master complete the communication. To write to the device again, repeat the entire write procedure; I<sup>2</sup>C burst write mode is not supported by the MAX9489.

### Reading the MAX9489 Setup

Reading from the MAX9489 registers begins with a START condition and a device address with the write bit set low, then the register address that is to be read, followed by a repeated START condition and a device address with the write bit set high, and finally the data are shifted out (Figure 4). Following a START condition, the first 7 bits comprise the device address. The 8th bit is low to indicate a write operation (to write in the following register address). An acknowledge bit is then generated by the MAX9489, signaling that it recognizes its address. The next 8 bits form the register address, indicating the location of the data to be read, followed by another acknowledge, again generated by the MAX9489. The master then produces a repeated START condition and readdresses the device, this time with the R/W bit high to indicate a read operation (Figure 4). The MAX9489 generates an acknowledge bit, signaling that it recognizes its address. The data byte is then clocked out of the MAX9489. A final not-acknowledge bit, generated by the master (not required), and a STOP condition, also generated by the master, complete the communication. To read from the device again, the entire read procedure is repeated; I<sup>2</sup>C burst read mode is not supported by the MAX9489.

### Device Control Registers

The MAX9489 has 17 control registers. The register addresses and functions are shown in Table 2. The first 16 registers are used to set the 15 outputs, with register 0x00 controlling all outputs simultaneously and the rest mapped to individual outputs. Register 0x10 accesses the frequency-margin control. All other addresses are reserved and are not to be used.



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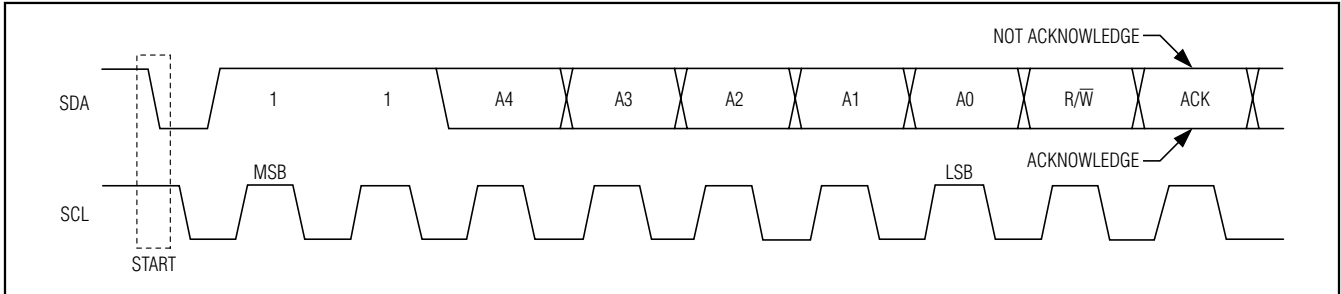


Figure 3. I<sup>2</sup>C Address and Acknowledge

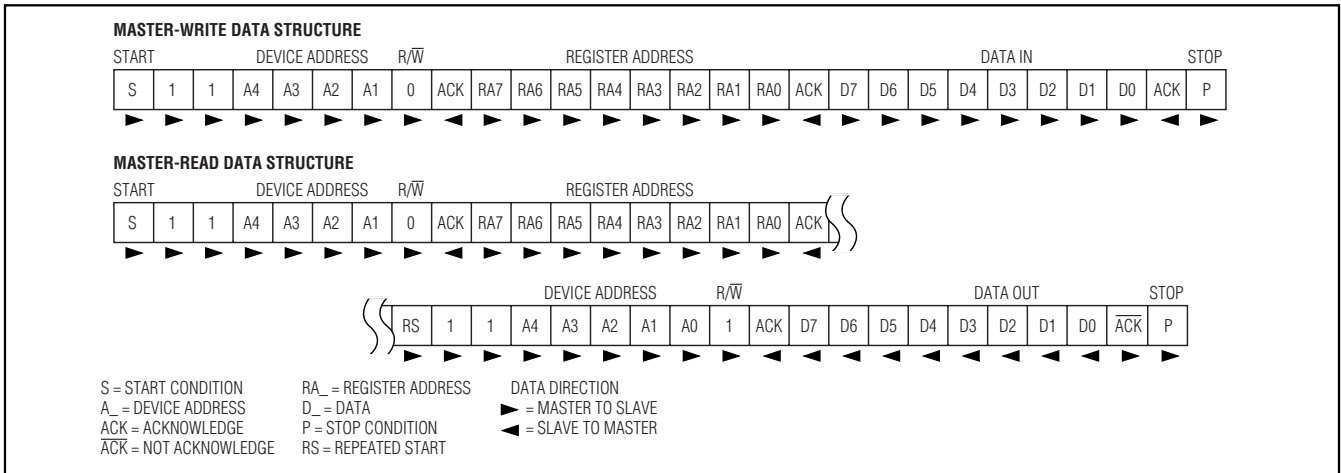


Figure 4. I<sup>2</sup>C Interface Data Structure

## Setting the Clock Frequencies

Each CLK<sub>n</sub> output has an associated control register. The contents of the registers determine the frequency of their associated outputs. Table 3 provides the frequency mapping for the registers.

Example: To program CLK3 to 80MHz, first address the device with R/W low, then send register address byte 0x03 followed by data byte 0x05 (Figure 5).

## Frequency Margin Control

Frequency margin is controlled through control register 0x10. Table 4 provides the mapping for the available margins. A selected margin applies to all outputs.

Example: To increase all clock outputs by 5%, address the device, then send register address byte 0x10 followed by data byte 0x01.

## Power Supply

The MAX9489 uses a 3.0V to 3.6V power supply connected to V<sub>DD</sub>, and 3.0V to 3.6V connected to AV<sub>DD</sub>.

Bypass each V<sub>DD</sub> at the device with a 0.1μF capacitor. Also bypass AV<sub>DD</sub> at the device with a 0.1μF capacitor. Additionally, use a bulk bypass capacitor of 10μF where power enters the circuit board.

## Board Layout Considerations

As with all high-frequency devices, board layout is critical to proper operation. Place the crystal as close as possible to X1 and X2, and minimize parasitic capacitance around the crystal leads. Ensure that the exposed pad makes good contact with GND.

## Chip Information

TRANSISTOR COUNT: 15,219  
PROCESS: CMOS

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**Table 2. Register Address Mapping**

| REGISTER ADDRESS BYTE | REGISTER FUNCTION              |
|-----------------------|--------------------------------|
| 0x00                  | Broadcast to all CLK registers |
| 0x01                  | CLK1                           |
| 0x02                  | CLK2                           |
| 0x03                  | CLK3                           |
| 0x04                  | CLK4                           |
| 0x05                  | CLK5                           |
| 0x06                  | CLK6                           |
| 0x07                  | CLK7                           |
| 0x08                  | CLK8                           |
| 0x09                  | CLK9                           |
| 0x0A                  | CLK10                          |
| 0x0B                  | CLK11                          |
| 0x0C                  | CLK12                          |
| 0x0D                  | CLK13                          |
| 0x0E                  | CLK14                          |
| 0x0F                  | CLK15                          |
| 0x10                  | Frequency margin control       |
| 0x11 – 0xFF           | Reserved, do not use           |

**Table 3. Output Frequency Control**

| CLK_ REGISTER DATA BYTE | OUTPUT FREQUENCY (MHz) |
|-------------------------|------------------------|
| 0x00                    | Logic low*             |
| 0x01                    | 133.3                  |
| 0x02                    | 125                    |
| 0x03                    | 100                    |
| 0x04                    | 83.3                   |
| 0x05                    | 80                     |
| 0x06                    | 66.6                   |
| 0x07                    | 62.5                   |
| 0x08                    | 50                     |
| 0x09                    | 33                     |
| 0x0A                    | 25                     |

\*Power-up default for CLK2 through CLK15.

**Table 4. Output Frequency Margin Control**

| MARGIN REGISTER DATA BYTE | OUTPUT FREQUENCY (MHz) |
|---------------------------|------------------------|
| 0x00                      | 0%                     |
| 0x01                      | 5%                     |
| 0x02                      | 10%                    |
| 0x07                      | -5%                    |
| 0x06                      | -10%                   |



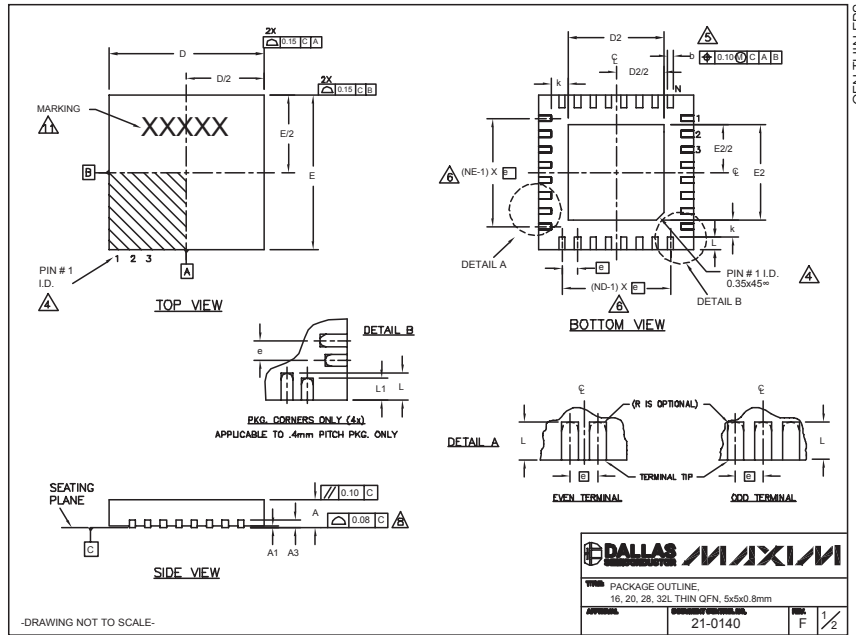
Figure 5. Example—Setting CLK3 to 80MHz

# Multiple-Output Network Clock Generator

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX9489



| COMMON DIMENSIONS |           |      |      |           |      |      |           |      |      |           |      |      |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG.              | 16L 5x5   |      |      | 20L 5x5   |      |      | 28L 5x5   |      |      | 32L 5x5   |      |      |
| SYMBOL            | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. |
| A                 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 |
| A1                | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 |
| A3                | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      |
| b                 | 0.25      | 0.30 | 0.35 | 0.25      | 0.30 | 0.35 | 0.20      | 0.25 | 0.30 | 0.20      | 0.25 | 0.30 |
| D                 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 |
| E                 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 |
| e                 | 0.80 BSC. |      |      | 0.65 BSC. |      |      | 0.50 BSC. |      |      | 0.50 BSC. |      |      |
| k                 | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    |
| L                 | 0.30      | 0.40 | 0.50 | 0.45      | 0.55 | 0.65 | 0.45      | 0.55 | 0.65 | 0.30      | 0.40 | 0.50 |
| L1                | -         | -    | -    | -         | -    | -    | -         | -    | -    | -         | -    | -    |
| N                 | 16        |      |      | 20        |      |      | 28        |      |      | 32        |      |      |
| ND                | 4         |      |      | 5         |      |      | 7         |      |      | 8         |      |      |
| NE                | 4         |      |      | 5         |      |      | 7         |      |      | 8         |      |      |
| JEDEC             | WHHB      |      |      | WHHC      |      |      | WHHD-1    |      |      | WHHD-2    |      |      |

| EXPOSED PAD VARIATIONS |      |      |      |      |      |      |       |                   |  |  |  |  |
|------------------------|------|------|------|------|------|------|-------|-------------------|--|--|--|--|
| PKG. CODES             | D2   |      |      | E2   |      |      | L     | DOWN BOWS ALLOWED |  |  |  |  |
|                        | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | ±0.15 |                   |  |  |  |  |
| T1655-1                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | NO                |  |  |  |  |
| T1655-2                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | YES               |  |  |  |  |
| T1655N-1               | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | NO                |  |  |  |  |
| T2055-2                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | NO                |  |  |  |  |
| T2055-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | YES               |  |  |  |  |
| T2055-4                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | NO                |  |  |  |  |
| T2055-5                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | 0.40  | Y                 |  |  |  |  |
| T2855-1                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | **    | NO                |  |  |  |  |
| T2855-2                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | **    | NO                |  |  |  |  |
| T2855-3                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | **    | YES               |  |  |  |  |
| T2855-4                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | **    | YES               |  |  |  |  |
| T2855-5                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | **    | NO                |  |  |  |  |
| T2855-6                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | **    | NO                |  |  |  |  |
| T2855-7                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | **    | YES               |  |  |  |  |
| T2855-8                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | 0.40  | Y                 |  |  |  |  |
| T2855N-1               | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | **    | N                 |  |  |  |  |
| T3255-2                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | NO                |  |  |  |  |
| T3255-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | YES               |  |  |  |  |
| T3255-4                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | NO                |  |  |  |  |
| T3255N-1               | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | **    | NO                |  |  |  |  |

NOTES:  
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.  
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.  
3. N IS THE TOTAL NUMBER OF TERMINALS.  
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.  
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.  
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.  
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.  
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.  
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.  
10. WARPAGE SHALL NOT EXCEED 0.10 mm.  
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.  
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

**DALLAS MAXIM**  
PACKAGE OUTLINE  
16, 20, 28, 32L THIN QFN, 5x5x0.8mm  
21-0140

-DRAWING NOT TO SCALE-

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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